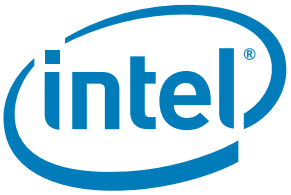

Troubleshooting IEEE Conformance Test Failures

January 2012

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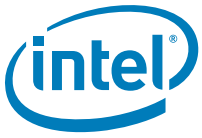
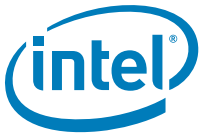
Revision 1.1



Contents

Revision History

Date	Revision	Description
January 2012	1.1	• Changed page size to 8 1/2 x 11. • Added new legal page.
December 2008	1.0	Initial public release.



1.0 Introduction

Readers of this application note will vary in familiarity with the subject matter from fairly new to those with a high degree of experience with it. This document assumes the reader is familiar enough with the IEEE Gigabit Physical Layer (PHY) test procedures to be able to recognize when an apparent test failure could be due to improper application of a test procedure and know how to re-check the setup and if necessary make appropriate adjustments and rerun it.

For readers just learning about IEEE Gigabit PHY conformance testing, this application note also provides information that includes checking test setups and measurement procedures where either or both are frequently found to cause false failure results as well as tips on the types of problems that can be caused by poor component choice or improper layout decisions. There is also some background information that many readers will know very well and can breeze over but the less experienced readers will find of interest

2.0 Scope

conformance testing of an Intel® LAN-based design (though many of the principles could be applied to any LAN design based on the 802.3 specification). This knowledge can help a designer by saving the time it takes to call customer support and/or the time it takes for a support engineer to understand the system design, which frequently requires a schematic review and possibly a layout review later on during troubleshooting. For this reason, it is highly recommended that a designer consult this application note when a problem occurs during Gigabit PHY conformance testing.

3.0 What is IEEE Gigabit PHY Conformance Testing?

PHY conformance testing is known to a majority of design engineers; however, some that are involved in this testing would find it difficult to define. In most cases, design engineers were taught the test procedures without explaining where it fits in the overall networking picture.

The 802.3 Ethernet specification provides the standards that an Ethernet device is required to meet. IEEE gigabit PHY conformance testing is the suite of tests used to test an Ethernet design to make sure it meets these standards from a gigabit PHY to the communication medium. For example, twisted pair, such as CAT-5 or CAT-6 cabling, tests is defined at the RJ45 connector. The 802.3 specification itself doesn't (with a few exceptions) define the conformance test methodology but since it does specify the electrical requirements, LAN silicon designers are able to develop their own test suites to meet the needs of their customer base as well as others who do testing for designers such as the University of New Hampshire's Interoperability Labs (UNH IOL). Additional information concerning UNH can be found at http://www.iol.unh.edu/services/testing/ge/ (and other sites as well).

Note: Signaling from a PHY (operating to specification) can be distorted by poor board layout, poor magnetics, inadequate power sources and clocks, and a variety of other nonrelated sources.

The intent of this application note is to make designers aware of these non-compliant sources so they can fix current and future Ethernet designs to meet specification compliance.

4.0 Why IEEE Gigabit PHY Conformance Testing?

To a potential customer, specification compliance indicates that the device has met the fundamental requirements for performing the basic network operations that are the foundation for network interoperability with other devices that conform to the standard.

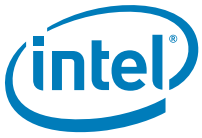
Without the first there is no guarantee the device will even communicate over the network infrastructure and without the second there is no guarantee it will be able to communicate reliably with the multitude of other devices on a typical network, even if it appears to be able to cover the design lab's test networking infrastructure to another device on that network.

Basic operation over a closed network might satisfy the needs of some designers (from a gigabit PHY perspective); however, others might need wide-scale interoperability. Note that wide-scale interoperability was recognized as networking development attracted the interest of a wide audience. This lead to a consortium of influential companies developing the 802.3 specification to define the standards the various components of a network must meet. Conformance testing verifies that a product conforms to the standard, a fundamental requirement for it to perform the basic networking operations. As previously mentioned, those who are interested only in basic networking operations over a closed network are mainly interested in certain basic tests while those who want to communicate reliably over something more complex (such as the Internet) need to perform far more comprehensive testing.

To test a design for compliance, two major requirements must be met: an external fixture that provides termination or connection for some of the compliance tests and the knowledge of how to put the PHY into the appropriate test modes.

A variety of test fixtures are available from a number of test equipment manufacturers. Make certain that when using these fixtures that you maintain short, reliable ground connections and provide the correct termination for the test you are running. Understand that some of the measurements can be affected by poor grounding or inappropriate termination.

When testing Intel Ethernet controllers, you can acquire a software tool through your Intel field application engineer or other Intel representative from Intel's LAN Access Division, LAN Conformance (LANConf), which will assist you in putting the PHY into the appropriate test modes to ensure correct testing. Accompanying manuals for both fast Ethernet and gigabit Ethernet provide details on the various tests such as their purpose, the measurement's specification and in most case examples of the waveforms taken from test equipment during performance of the test being explained; not representative drawings but the test's actual waveforms. These manuals also list the required test fixtures along with directions for their construction, saving designers the cost of purchasing commercial versions, and the required test equipment to run the test software and to take the actual measurements that indicate if the Unit Under Test (UUT) passes the tests.



LANConf is available in DOS, both 32-bit and 64-bit versions of Linux, Windows and EFI and is part of Intel's tools package for Intel Ethernet controllers. This includes a number of other valuable tools for programming EEPROMs in an automated fashion along with many other EEPROM related functions and tests, performing operational diagnostic testing of LAN on Motherboard (LOM) and LAN adapter designs, and a

number of other valuable tools for designers and the OEM. LANConf can be downloaded from CDI or MySMG. LANConf is part of our tools package for Intel Ethernet controllers, also including valuable tools like EEUPDATE and CELO.

The monolithic PXE image is relatively large, so this means even if the BIOS supports PMM, it has to have that much free space just to begin option ROM initialization. By using a split ROM, the PXE base code is broken out into its own option ROM image. Now there are two option ROMs that need to be initialized. The Boot Agent split ROM consists of two modules, each of which is smaller than the monolithic image. The combined size of the two is greater, but the BIOS requires less free space to initialize each one. Each image also shrinks after initialization. The final result is that it is takes up a little more space in upper memory at boot time but doesn't take as much during initialization.

The monolithic and split Init/UNDI images are PCI 3.0 compliant and can be loaded in conventional memory during initialization. The split base code image is still PCI 2.x compliant and must be loaded into the UMB.

5.0 How to Use This Document

This document should be used as a support document that provides next step direction for debugging a failed design. It can also be used by designers that are starting a design with Ethernet involved and want to become aware of pitfalls of certain design decisions they might make during layout or component selection for this design. Both those starting a design and those having problems during conformance testing should know that Intel provides design guides for each LAN controller. These design guides provide detailed information on the layout, component selections, termination resistor and capacitor values, and detailed design and troubleshooting information. The ideal is to follow the design guide for the Intel LAN component being used; however, for those who didn't have that opportunity should obtain it as it can help explain what might have been done wrong for each of listed compliance failures (described later) assuming it is due to the design and not improper testing. For the latter, the manuals that were previously mentioned detailing the test setup and measurements techniques should be consulted as well as this document.

When a failure is observed during IEEE conformance testing the first step for any test is to verify that the setup is correct and the method being used to obtain the results is being performed correctly. Many have spent long hours attempting to fix a problem on their design that turned out to be due to a poorly designed test setup or incorrect testing. Always examine the setup carefully, verify calibration, settings, connections and such. It is better to spend an hour, if needed, to ensure your setup and test methodology is correct than attempt to troubleshoot a non-existent problem with your design. This is even more critical if previous boards have been passing. In that case, if available, a quick check is to retest one of the passing boards and see it now fails. If it does then it is more likely the test setup has been compromised.

Another item to consider is a previously passing design that has been modified but is still quite similar. By examining the areas of the LAN design that have been changed might help identify the possible cause of the failure such as the distance from the PHY to the connector was increased to far, an incorrect value component was incorporated, etc. Again, careful examination of these areas can save a lot of time finding the problem.

6.0 IEEE Compliance Failures and Possible Sources of Failure

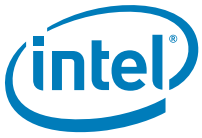
Following is a chart that has been compiled from years of Ethernet compliance testing of Intel designs with Intel Ethernet silicon. The first column indicates the category of IEEE compliance test that might have failed. The row corresponding to that test indicates the possible source of the failure in that design with an X. A decoder for #1-15 can be found in the chart that follows.

Catagory	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Output Amplitude	X	X	X	X	X	X										X
Output Templates	X		X				X	X	X	X						X
CMR	X		X					X			X	X	X			X
Return Loss	X	X	X				X	X	X	X	X					X
Rise/Fall Times	X		X				X				X	X				X
Jitter	X		X					X			X		X	X	X	X
BER	X	X	X									X		X	X	X

1. The AFE (analog front end) is too long.
2. There are incorrect values of termination resistors in the design.
3. The test has been run with a low quality or faulty magnetic.
4. R-Bias resistor(s) have incorrect value(s).
5. There is no resistor on magnetic center tap (line-side).
6. Is this a trimmed component (82541x/82547x specific)?
7. There might be trace stubs on the AFE.
8. The MDI traces are not routed differentially the entire way.
9. There might be inductors on the MDI traces.
10. There might be capacitors installed on the MDI traces.
11. The intra-pair lengths are not matched.
12. Is there a capacitor on the magnetic center taps?
13. Is there a ground plane under the MDI pairs?
14. The crystal (or oscillator) is not stable (should be +/-50 ppm or better).
15. The power supply for the Ethernet controller and PHY-side center tap of the magnetics might not be stable or quiet.
16. Test equipment setup and use.

For example, if you have a design that fails Common Mode Rejection (CMR) tests, you should look at your AFE, the distance between your PHY and magnetics, revisit the quality of your magnetics and the vendor specifications that need to be met, layout with respect to your MDI pairs on the design, matching inter-pair lengths for the MDI pairs, the presence of a center tap capacitor, as well as the board stack-up where a ground reference plan is best case for the layer under the MDI traces.

These 15 possible sources of failures are detailed in the following sections. Designers need to make sure that the failures are well understood so they can be avoided in existing/future designs.



1. **The AFE (analog front end) is too long.**

AFE consists of termination components, the RJ45 connector, silicon output buffers, magnetics, and traces. AFE performance is highly design dependent; each design is slightly different and each design presents a new problem. Again, the design guide for the particular Intel LAN silicon provides valuable information on designing this section properly. In general, keep the total distance from the PHY to the connector short, at least one inch but not more than four inches. If the LAN silicon is too close to the connector, then some of its radiated EMI might couple onto the connector shield possibly causing excessive radiated EMI at the LAN cable, which can create other problems (discussed later in this document).

2. **There are incorrect values of termination resistors in the design.**

Examine the termination resistor specification for the Ethernet controller you are working with. Intel specifies a range of values across our product line. In fact, some of our newer devices have the termination resistors embedded in the devices.

If you are correctly using the value specified in the design guide and datasheet, consider a slightly lower value (-10%) for better return loss or a higher value (+10%) for better Bit Error Rate (BER).

3. **The test has been run with a low quality or faulty magnetic.**

Even though a magnetic (transformers) might be datasheet equivalent does not mean their quality and reliability is equivalent. Unlike silicon, the manufacturing is less controlled and is truly little wires being wrapped around toroid cores. ODMs always try to push for cheaper design.

Magnetics selection is the number one cause of IEEE test failures at late stages of product development (over 50%) so do not try to save money here! Test at least several samples for proper function from two or three different lots from the same manufacturer. The more samples and different lots the greater the likelihood of getting a magnetics that works well but there's a trade-off of the time it takes to test and getting the design finished so three to five samples from two to three lots should give a good indication assuming they all function well.

Please be aware that although Intel LAD provides a list of tested magnetics in each design guide that does not mean they have been qualified. We neither qualify magnetics nor do we recommend any specific brand for use with our devices. The ones we list as tested mean just that; we used them successfully in one or more designs but that in no way guarantees they will work in another design. However, it does indicate a good chance that they are compatible with the LAN controller they were tested with but that is all.

4. R-Bias resistor(s) is/are of incorrect value(s).

This is where the datasheet or design guide, whichever has the R-Bias resistor values specified, for the LAN controller is really necessary. For gigabit Ethernet controllers, most of Intel's have set bias resistor values and it is recommended not to change them.

Doing so can cause the design to be considered out of our specification and therefore not supported. With our Fast Ethernet (10/100 Mb/s) controllers however, the datasheet specifies a starting value and a note indicating it is a starting value. Caution is still needed as the recommended starting value has been determined by much testing of different designs and is a value that works quite well in the majority of customer designs; so well in fact there are no formulae or suggestions given on how to determine a new value so before tweaking it be sure it is necessary. If it is determined to be necessary make small value changes on the order of 20 to 30 ƒÇ at a time. Increases reduce the output peak-to-peak amplitude while decreases increase the amplitude. In both cases if the changes were made for some reason after IEEE conformance testing it is necessary to redo the differential transmit voltage tests to be sure they are still within the specification's requirements.

5. There is no resistor on magnetic center tap (line-side).

A Bob Smith termination is often provided for the media-side center-taps. This circuit is used to enhance EMI and ESD performance of the system, specifically Common Mode Noise (CMM).

6. Is this a trimmed component (82541x/82547x specific)?

Certain versions of the 82541x and 82547x devices have been trimmed as a means of correcting certain design errata. Contact your Intel representative if you encounter device certification issues with the 82541x and 82547x controller families.

7. There might be trace stubs on the AFE (mainly mobile platforms).

Stubs can be found in mobile designs that use LAN switches and docking stations to accomplish their design. Other designs that might have trace stubs are those designed for use in multiple environments. In certain very noisy environments that mainly embedded designs are used in, the requirements for the board might include having pads and trace stubs to place transient protection diode packs to protect the board's circuitry from spikes. When used where such protection is not a requirement, the packs are not placed leaving just the pads and traces stubs. Stubs on the transmission lines can add extra capacitive loading and if they're on a specialty mobile platform it is possible to have both stubs for LAN switches and protective diodes. If required, keep the traces as short as possible and use the absolute minimum necessary. Stubs on the transmission lines between the silicon and the magnetics are the number one cause of return loss failures so if your design fails return loss consistently and you have such stubs see if you can remove any or shorten them and your routes from the PHY to the magnetics. Also route the lines from the silicon to the magnetics with extra care, preferably by hand to control the differential impedance as closely as possible.

8. The MDI traces are not routed differentially the entire way.

Layout guidelines for differential traces:

a. Keep the two traces in a differential pair equal in length and close together.

b. Keep the two traces in a differential pair symmetric.

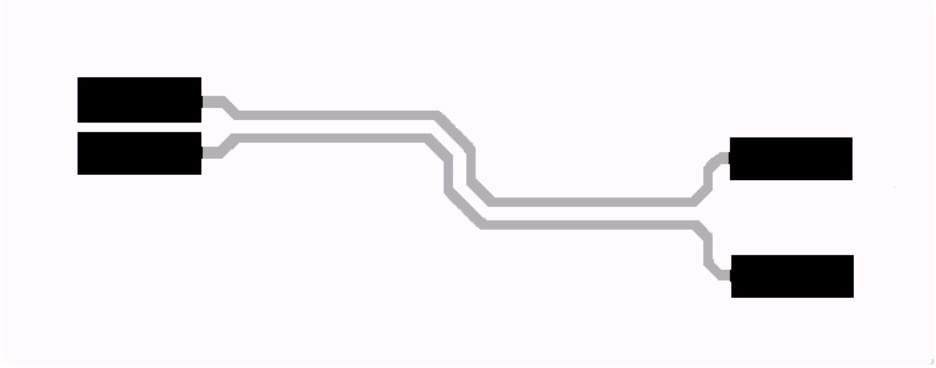


Figure 1. Correct MDI Trace Routing

Or

Figure 2. Incorrect MDI Trace Routing

Note: TDR the traces for 100 Ω differential.

9. There may be inductors / capacitors on the MDI traces.

Adding capacitive and/or conductive components to the MDI traces changes the characteristics of trace impedance. Please remove these. If ESD suppression diodes are required for you design, choose low capacitance (<5 pf) devices.

10. There may be inductors / capacitors on the MDI traces.

Adding capacitive and/or conductive components to the MDI traces changes the characteristics of trace impedance. Please remove these. If ESD suppression diodes are required for you design, choose low capacitance (<5 pf) devices.

11. The intra-pair lengths are not matched.

Inside an MDI pair, the lengths of each of those traces need to be matched within 50 mils. Please check this in your layout.

12. Is there a capacitor on the magnetic center taps?

Make sure there is a bypass capacitor (typically 0.01 µF) on all PHY side center taps of the magnetics. Do not use one large cap: use one bypass capacitor for each center tap.

13. Is there a ground plane under the MDI pairs?

Board stack up can be a contributor to poor performance. Ideally, the signal layer that routes the MDI pairs is in between two ground planes, offering the best noise isolation. The worse case that can be offered is that the MDI signal layer is next to another signal layer that has other high speed traces that run parallel to the MDI pairs. This offers the opportunity for broadside coupling between these adjacent signal; not a desired effect. Follow the layout and design checklists offered to you for each Intel Ethernet controller to avoid poor board stack up.

14. The crystal (or oscillator) is not stable (should be +/-50 ppm or better).

Clock stability and accuracy can always affect signal quality. Make sure that your clock meets accuracy and jitter specifications that are called out in the device datasheet. If you are using a crystal, make sure the external load capacitors meet the recommended values that are provided in the datasheet or have a good reason for why they do not. If you are providing a clock using an oscillator, make sure your V dc offset is correct and the amplitude of the clock is appropriate for the Ethernet device you are using. Also keep in mind that most generic oscillators are only rated for 100 ppm accuracy: out of specification for use in a Ethernet application.

15. The power supply for the Ethernet controller and PHY side center taps of the magnetics might not stable or quiet.

Does the supply meet the tolerance and ripple specifications provided in the datasheet? Do you provide decoupling at the source of the supply and at the point where voltage is supplied to the chip? Check the quality of the center tap supply.

Three key needs for creating power supplies for use with Intel Ethernet controllers:

- Use metal grounds to create a heat sink effect for regulators to dissipate heat.
- Connect each voltage regulator's fill layers with multiple thermal VIAs.
- Make sure to use decoupling capacitors NEAR the inputs to the Intel LAN controller.

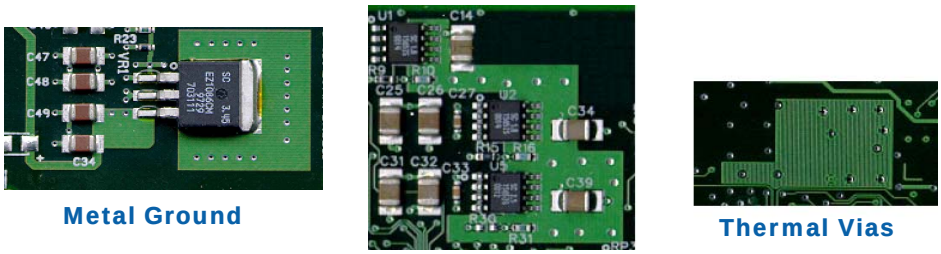


Figure 3. Needs for Creating Power Supplies

16. Test Equipment not set up correctly.

Test equipment set up, fixturing, and signal grounding is one of the most overlooked failure contributor of all. Be mindful of the signals that you are measuring. Troubleshoot your fixtures and make sure they offer you with the appropriate termination, connection, and ground isolation. Make sure that your ground connections are short and robust.

7.0 Summary

IEEE testing and self-compliance can be a good indication of the robustness and specification compliance of your designs. Remember these tips:

1. Intel design guides, datasheets, and schematic and layout checklists can be found under the Ethernet component section of developer.intel.com.
2. Use tested magnetics for your design. Over 50% of failures are due to out of specification magnetics.
3. Consider using Intel's software tools - Tools like LANConf can assist in your tests and minimize software effort that is involved in performing IEEE tests.
4. Use Intel for schematic and layout reviews - Intel provides One Time Schematic Review (OTSR) services free of charge to customers of our Ethernet controllers. Please use our expertise to save you schedule time and design effort with respect to Ethernet.